Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 5-10, 16-20, and 26-31. Please amend claims 1-3, 11-13, 21-23, 32, 36, and 40, as follows:

Listing of Claims:

1. (Currently amended) A memory hub for a hub-based memory module, the memory hub configured to be coupled to a bidirectional data bus operable to transfer both read and write data, the memory hub comprising:

first and second link interfaces for coupling to respective portions of the data bus[[ses]]; and

a data path coupled to the first and second link interfaces, the data path having a direct data path [[and]] through which data is transferred between the first and second link interfaces and further having a bypass data path, the bypass data path having [[; and]]

a write bypass circuit coupled to the direct data path and operable to couple write data on the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path.

2. (Currently amended) The memory hub of claim 1 wherein the write bypass circuit comprises:

a multiplexer having a first input coupled to the direct data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the direct data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

3. (Currently amended) The memory hub of claim 2 wherein the write bypass circuit further comprises an input buffer having an input coupled to the direct data path and an output coupled to the inputs of the multiplexer and the FIFO register.

4. (Original) The memory hub of claim 1, further comprising a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

5-10. (Cancelled)

11. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices and configured to be coupled to a bidirectional data bus operable to transfer both read and write data, the memory hub comprising:

first and second link interfaces for coupling to respective portions of the data bus[[ses]]; and

a data path coupled to the first and second link interfaces, the data path having a direct data path [[and]] through which data is transferred between the first and second link interfaces and further having a bypass data path, the bypass data path having [[; and]]

a write bypass circuit coupled to the direct data path and operable to couple write data on the direct data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path.

12. (Currently amended) The memory module of claim 11 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the direct data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the direct data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

13. (Currently amended) The memory module of claim 12 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the direct data path and an output coupled to the inputs of the multiplexer and the FIFO register.

14. (Original) The memory module of claim 11 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

15. (Original) The memory module of claim 14 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

16-20. (Cancelled)

21. (Currently amended) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices and configured to be coupled to a bidirectional data bus operable to transfer both read and write data, the memory hub comprising:

first and second link interfaces for coupling to respective portions of the data bus[[ses]]; and

a data path coupled to the first and second link interfaces, the data path having a direct data path [[and]] through which data is transferred between the first and second link interfaces and further having a bypass data path, the bypass data path having [[; and]]

a write bypass circuit coupled to the direct data path and operable to couple write data on the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path.

22. (Currently amended) The processor-based system of claim 21 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the direct data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the direct data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

23. (Currently amended) The processor-based system of claim 22 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input

coupled to the direct data path and an output coupled to the inputs of the multiplexer and the FIFO register.

24. (Original) The processor-based system of claim 21 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

25. (Original) The processor-based system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

26-31. (Cancelled)

32. (Currently amended) A method for writing data to a memory location in a memory system coupled to a bidirectional memory bus transmitting both read and write data, comprising:

accessing read data in the memory system;

providing write data to the memory system on the bidirectional memory bus;

coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written;

coupling the read data to the bidirectional memory bus and providing the read data for reading;

coupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

33. (Original) The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. (Original) The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. (Original) The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. (Currently amended) A method for executing memory commands in a memory system having a memory bus on which both read and write data can be coupled, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data for the write command to the memory bus of the memory system after issuing the read command;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. (Original) The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. (Original) The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. (Original) The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. (Currently amended) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.